STIC Search Report
EIC 2800

STIC Database Tracking Number: 131654

TO: Monica Lewis Location: JEF-5A30 September 20, 2004 AU 2822 Case Serial No. : 09/939,457	From: Jeff Harrison Location: STIC-EIC2800 JEF-4B68 Phone: 22511 Email: harrison, jeff

Search Notes

Examiner Lewis,

Re: Protruding electrodes, conductive film on top, insulating resin on side

Attached are edited results from patent and nonpatent literature.

If you'd like additional searching or explanation, let me know.

Respectfully,
Jeff

Jeff Harrison
Team Leader, STIC-EIC2800
JEF-4B68, 571-272-2511

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JEF-4B68, 571-272-2511

FILE 'HCAPLUS, WPIX' ENTERED AT 15:20:06 ON 20 SEP 2004

```
L1             2    S    US20020048905/PN
L2               SEL PLU=ON  L1 1- IC RN :      12 TERMS
L3         97779    S    L2
L4             2    S    L1 AND L3
L5               SEL PLU=ON  L4 1- IC MC :      13 TERMS
L6        410401    S    (MEMBRAN##### OR FILM OR LAYER OR SUBLAYER
                 OR COAT####)(3A)(ELECTRODE OR CONDUCT#######)
L7           397    S    (PROTRU#### OR PROMINEN#### OR PROTUB#####)  (5A) BUMP
L8             0    S    (PROTRU#### OR PROMINEN#### OR PROTUB#####)  (5A) BALLBUMP
L9             1    S    (PROTRU#### OR PROMINEN#### OR PROTUB#####) (5A) GLOB
L10         7543    S    (PROTRU#### OR PROMINEN#### OR PROTUB#####)(5A) CONTACT
L11         1012    S    (PROTRU#### OR PROMINEN#### OR PROTUB#####) (5A) PAD
L12        10370    S    (PROTRU#### OR PROMINEN#### OR PROTUB#####)(5A)(ELECTRODE OR CONDUCT##### OR
METAL##############)
L13           66    S    (PROTRU#### OR PROMINEN#### OR PROTUB#####) (5A)(CONDUCTIVE OR CONDUCTING OR
METAL#######)(W) FILM
L14        29210    S    (NONCONDUCT####### OR NON CONDUCT OR NON ELECTRICALLY CONDUCT###### OR
INSULAT#########)(3A) RESIN######
L15          193    S    RESIN####(5A)(SIDE## OR LATERAL###)(4A)(PROTRU#### OR PROMINEN#### OR
PROTUB#####)
L16         1543    S    L6 AND (L7 OR L8 OR L9 OR L10 OR L11 OR L12 OR L13)
L17         1543    S    L6 AND (L7 OR L8 OR L9 OR L10 OR L11 OR L12)
L18           34    S    L17 AND L13
L19            1    S    L18 AND L14
L20            1    S    L18 AND L15
L21       101494    S    L5
L22            8    S    L18 AND L21
L23           34    S    L18 AND L6
L24         1543    S    L6 AND (L7 OR L8 OR L9 OR L10 OR L11 OR L12 OR L13) AND (L14 OR L15 OR L16 OR
L17 OR L18)
L25         1298    S    L24 AND (PROTRU#### OR PROMINEN#### OR PROTUB#####)(5A)(CONDUCT###### OR
ELECTRODE)
L26          150    S    L25 AND RESIN
L27           23    S    L26 AND (CONDUCT####### OR METAL####### OR FILM)(4A)(OBVERSE OR REVERSE OR
OTHER OR BOTTOM OR SIDE OR LOWER OR REAR OR BEHIND OR OTHER)
L28            3    S    L26 AND (CONDUCT####### OR METAL####### OR
                 FILM)(4A)(BACK OR BACKSIDE)
L29            2    S    L26 AND (TWO OR THREE OR FOUR OR SEVERAL OR PAIR## OR COUPLE OR MATRIX#### OR
ARRAY##### OR LINE OR ROW OR COLUMN)(2A) BUMP
L30        15781    S    (PROTRU#### OR PROMINEN#### OR PROTUB#####)(3A)(TWO OR THREE OR FOUR OR SEVERAL
OR PAIR## OR COUPLE OR MATRIX#### OR ARRAY##### OR LINE OR ROW OR COLUMN)
L31            7    S    L6 AND L7 AND (RESIN#### OR EPOX#### OR NOVOLAK OR
POTTING)(4A)(NONCONDUCT###### OR NON CONDUCT### OR INSULAT####)
L32            9    S    L26 AND L30
L33           73    S    L9 OR (L18 OR L19 OR L20) OR L22 OR L23 OR (L27 OR L28 OR L29) OR (L31 OR L32)
L34       101502    S    L5
L35           20    S    L34 AND L33
L36            9    S    L33 AND INTERCONNECT?
L37            7    S    L33 AND BUMP AND RESIN AND FILM
L38           34    S    L9 OR L19 OR L20 OR L22 OR L28 OR L29 OR L31 OR L32 OR L36 OR L37
L39            9    S    L27 AND L35
L40           36    S    L38 OR L39
L41           36    S    L40 NOT L4
```

FILE 'JAPIO, INSPEC, EUROPATFULL, PCTFULL' ENTERED AT 15:48:11 ON 20 SEP 2004

```
L42         2344    S    (PROTRU#### OR PROMINEN#### OR PROTUB#####)(4A)(BUMP OR CONTACT OR
ELECTRODE)/TI,AB,CLM,CT,ST
L43          408    S    (PROTRU#### OR PROMINEN#### OR PROTUB#####)(4A)(BUMP OR CONTACT OR
ELECTRODE)/AB
L44           18    S    (L42 OR L43) AND (FILM OR TOP)(3W)(PROTRU#### OR PROMINEN#### OR PROTUB##### OR
BUMP)/TI,AB
L45            0    S    L44 AND (RESIN#### OR EPOX##### OR POTTING OR NOVOLAK)(4A)(CONTACT#### OR SIDE
OR LATERAL###)(3A)(BUMP OR ELECTRODE OR PROTRU#### OR PROMINEN#### OR PROTUB#####)/TI,AB
L46            9    S    L44 AND (FILM OR LAYER OR MEMBRAN####)(2A)(CONDUCT### OR ELECTRODE)
L47            1    S    L44 AND INTERCONNECT#####/TI,AB,ST,CT,CLM
L48            3    S    L44 AND (RESIN#### OR EPOX##### OR POTTING OR NOVOLAK)/TI,AB,CLM,ST,CT
L49           10    S    (L46 OR L47 OR L48)
```

131654

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 3/15/2004 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, JEF-4B68, 272-2511.

Date 9/2/04 Serial # 09/939,457 Priority Application Date _____

Your Name M. Lewis Examiner # _____

AU 2899 Phone 272-1838 Room 5A30

In what format would you like your results? Paper is the default. PAPER DISK EMAIL

Need before 9/16

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: 9-03-[illegible] 9:19

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____

Secondary Refs ✓ Foreign Patents ___

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-5

Problem: See pages 1-3

Solution: " " " 4

protruding electrodes

Staff Use Only		Type of Search		Vendors	
Searcher:	HARRISON	Structure (#)		STN	X
Searcher Phone:	22511	Bibliographic	X	Dialog	
Searcher Location:	STIC-EIC2800. JEF-4B68	Litigation		Questel/Orbit	
Date Searcher Picked Up:	9-20-04	Fulltext	X	Lexis-Nexis	
Date Completed:	9-20-04	Patent Family		WWW/Internet	
Searcher Prep/Rev Time:	45	Other		Other	
Online Time:	35				

L41 ANSWER 5 OF 36 HCAPLUS COPYRIGHT ACS on STN
AN 1995:708435 HCAPLUS Full-text
DN 123:99795
ED Entered STN: 29 Jul 1995
TI Electric conductor - **insulator resin** composites and circuit boards
IN Azuma, Kazumi; Maeda, Masako
PA Nitto Denko Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H05K001-02
ICS H05K001-03; H05K003-46
ICA H05K001-11
CC 76-2 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 07030212	**A2**	**19950131**	**JP 1993-169342**	**19930708**
PRAI JP 1993-169342		**19930708**		

CLASS

PATENT NO.	CLASS	PATENT FAMILY CLASSIFICATION CODES
JP 07030212	ICM	H05K001-02
	ICS	H05K001-03; H05K003-46
	ICA	H05K001-11

AB Through holes are formed in **insulator resin films** (e.g., polyimide) covered with elec. **conductive films** (e.g., Cu foils), and metals are **protruding bump**-like from the holes. Plastic **films** may be formed on the **resin films** on the opposite side of the elec. **conductive films**. The elec. **conductive films** may be patterned into elec. circuits, or the composite **films** are laminated, and the interlayer circuits are connected across the holes.
ST elec conductor insulator composite circuit board; copper polyimide composite circuit board
IT Polyimides, uses
RL: DEV (Device component use); USES (Uses)
(elec. conductor - **insulator resin** composites and circuit boards)
IT Electric circuits
(printed, boards, elec. conductor - **insulator resin** composites for)
IT 7440-50-8, Copper, uses
RL: DEV (Device component use); USES (Uses)
(elec. conductor - **insulator resin** composites and circuit boards)

L41 ANSWER 6 OF 36 HCAPLUS COPYRIGHT ACS on STN
AN 1993:615340 HCAPLUS Full-text
DN 119:215340
ED Entered STN: 13 Nov 1993
TI Anisotropic electrically **conductive film**, and method for connecting electronic devices by using such film
IN Kobayashi, Hiroshi; Yoshida, Yoshihiro; Kozuka, Takeshi; Iwabuchi, Toshiaki
PA Ricoh Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01R011-01
ICS C08K003-08; C08L101-00; H01B005-16; **H05K003-32**
CC 76-2 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI	**JP 05047428**	**A2**	**19930226**	**JP 1991-201000**	**19910812**
				JP 1991-201000	19910812

CLASS

PATENT NO.	CLASS	PATENT FAMILY CLASSIFICATION CODES
JP 05047428	ICM	H01R011-01
	ICS	C08K003-08; C08L101-00; H01B005-16; **H05K003-32**

AB In a porous insulating film (especially, anodized Al film) having a plurality of through openings containing **electrodes**, the **electrodes protrude** from the **film** surface and consist of a metal matrix having high oxidation resistance (e.g., Au and Ni) and dispersed hard particles (e.g., A2O3 and SiC) having hardness higher than that of the contacts of elec. devices to be connected. Elec. devices are connected by placing the film between them and applying ultrasonic wave. The hard particles destroy the oxidation film present on the contacts of the elec. devices thus providing for reliable elec. contact.

ST anisotropic elec **conductive film**; gold alumina composite elec contact; connecting elec device film ultrasonic wave

IT Electric contacts
(composite, of gold or nickel matrix with alumina or silicon carbide hard particles, in anisotropic elec. **conductive film** for connecting elec. devices)

IT Sound and Ultrasound
(in connecting elec. devices by using anisotropic elec. **conductive film**)

IT **Films**
(elec. **conductive**, anisotropic, with **protruding** composite **contacts** for connecting elec. devices)

IT Electric conductors
(**interconnections**, with anisotropic elec. **conductive film** with **protruding** composite **contacts** for, for elec. apparatus)

L41 ANSWER 14 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN

AN 2002-237016 [29] WPIX Full-text

CR 2001-366493 [38]; 2001-488377 [53]; 2002-089225 [12]; 2002-341542 [38]; 2002-488845 [52]; 2002-626277 [67]; 2002-749686 [81]

DNN N2002-182324 DNC C2002-071686

TI Semiconductor device for mounting on substrate, includes chip provided with bonding pads, in which conductive bodies are transferred to pad mounting surface to establish electrical connection of bonding pads and solder points.

DC L03 U11

IN CHEN, I

PA (CHEN-I) CHEN I

CYC 1

PI US 6333561 B1 20011225 (200229)* 9 H01L023-48 <--

ADT US 6333561 B1 US 2000-564989 20000505

PRAI TW 2000-100578 20000121

IC ICM **H01L023-48**
ICS H01L023-40; **H01L023-52**

AB US 6333561 B UPAB: 20030820
NOVELTY - Semiconductor device comprises a semiconductor chip having a pad-mounting surface provided with bonding pads. Conductive bodies are transferred from a conductor-forming mold to the pad mounting surface, to establish the required electrical connection among the bonding pads and the solder points.

DETAILED DESCRIPTION - A semiconductor device for mounting on a substrate (9) having a chip-mounting region with solder points, comprises a semiconductor chip. The chip has a pad-mounting surface (10) provided with bonding pads (11) at locations that are offset from locations of corresponding solder points on the chip-mounting region. Conductive bodies have extension portion which is electrically connected to respective bonding pads. The bodies have an electrical connection portion which is formed on an end of the extension portion. The conductive bodies are formed by providing a **conductor**-forming mold having a **side** formed with **conductor**-receiving cavities. The cavities include a first cavity part which is disposed in the conductor-forming

mold. The conductor-receiving cavities are filled with a conductive metal paste (91) to form the conductive bodies. The extension portions of the conductive bodies are disposed in the first cavity parts of the conductor-receiving cavities. The electrical connection portions of the conductive bodies are disposed in the second cavity parts of the conductor-receiving cavities. The conductive bodies are transferred from the conductor-forming mold to the pad-mounting surface of the semiconductor chip, through a transfer printing unit.

USE - For mounting on a substrate.

ADVANTAGE - Prevents the occurrence of short-circuiting due to the relatively short distance between bonding pads.

DESCRIPTION OF DRAWING(S) - The figures show a sectional view and a fragmentary schematic view of the semiconductor device.

insulator barriers 8

substrate 9

pad-mounting surface 10

bonding pads 11

conductive metal paste 91

Dwg.9,11/11

TECH US 6333561 B1 UPTX: 20020508

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: Insulator barriers (8) are formed on the pad-mounting surface, between an adjacent pair of the bonding pads. Conductive balls are disposed on the electrical connection portion of the **conductive** bodies. A protective **layer** made of an insulator material, is formed on the pad-mounting surface of the chip. The **conductive** balls **protrude** through the protective layer.

TECHNOLOGY FOCUS - POLYMERS - Preferred Material: The insulator barriers and the protective layer are formed from a **resin** material.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The conductive balls are copper balls electroplated with a conductive metal material. The conductive metal paste contains silver, gold, copper, iron, aluminum, tin, and lead.

L41 ANSWER 15 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN

AN 2002-165697 [22] WPIX Full-text

CR 2002-084295 [12]; 2002-488559 [52]; 2003-864465 [80]

DNN N2002-126522

TI Slim-line circuit board for portable devices e.g. mobile telephones, uses epoxy **resin** to support conductive tracks.

DC T01 U11 W01

IN KOBAYASHI, Y; MAEHARA, E; MASHIMO, S; OKAWA, K; SAKAMOTO, J; SAKAMOTO, N; TAKAHASHI, K

PA (SAOL) SANYO ELECTRIC CO LTD; (KOBA-I) KOBAYASHI Y; (MAEH-I) MAEHARA E; (MASH-I) MASHIMO S; (OKAW-I) OKAWA K; (SAKA-I) SAKAMOTO J; (SAKA-I) SAKAMOTO N; (TAKA-I) TAKAHASHI K

CYC 30

PI	**EP 1122778**	**A2**	**20010808 (200222)* EN**	**32**	**H01L023-31**
	R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI				
	JP 2001217338	A	20010810 (200222)	15	H01L023-12
	JP 2001217353	A	20010810 (200222)	15	H01L023-28
	JP 2001217372	A	20010810 (200222)	15	H01L023-50
	JP 2001223317	A	20010817 (200222)	18	H01L025-04
	JP 2001223318	A	20010817 (200222)	17	H01L025-04
	JP 2001223320	A	20010817 (200222)	19	H01L025-04
	KR 2001078000	A	20010820 (200222)		H05K001-02
	CN 1343086	A	20020403 (200247)		H05K001-00
	US 6548328	B1	20030415 (200329)		H01L021-44
	US 2003151135	A1	20030814 (200355)		H01L029-74
	US 2003160317	A1	20030828 (200357)		H01L023-48
	TW 535462	A	20030601 (200374)		H05K001-00

PRAI JP 2000-32454 20000209; JP 2000-22646 20000131;
JP 2000-24047 20000201; JP 2000-32417 20000209;
JP 2000-194094 20000131; JP 2000-194093 20000209

IC ICM H01L021-44; H01L023-12; H01L023-28; H01L023-31; H01L023-48; H01L023-50; H01L025-04; H01L029-74; H05K001-00; H05K001-02
ICS H01L021-301; H01L021-48; H01L021-50; H01L021-56; H01L025-00; H01L025-10; H01L025-11; H01L025-18; H01L031-111; H05K001-18; H05K003-30

AB EP 1122778 A UPAB: 20031211
NOVELTY - The slim-line circuit board has semiconductor components mounted on pressed metal i.e. copper, conductive paths that are supported in a glass epoxy **insulating resin** substrate. The paths are **conductively coated** with gold, silver or nickel. External connections are made via **protruding conductive** elements on the circuit **back** face.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is made for a method of manufacturing a circuit board.
USE - Slim-line circuit boards for use in portable equipment such as mobile telephones or laptop computers.
ADVANTAGE - The manufactured circuit boards are lighter in weight and thinner in profile.
Dwg.0/29

TECH EP 1122778 A2 UPTX: 20020409
TECHNOLOGY FOCUS - POLYMERS - The conductive tracks are supported in a glass epoxy **resin** substrate.

L41 ANSWER 16 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN

AN 2002-121269 [16] WPIX Full-text
DNN N2002-090951 DNC C2002-037021
TI Semiconductor device has semiconductor substrate including signal pads and ground pads, insulating **film, conductive** metal **film**, and first **interconnection** lines.
DC A85 L03 U11
IN FUKASAWA, N; IKUMO, M; KAWAHARA, T; NAGASHIGE, K
PA (FUIT) FUJITSU LTD; (FUKA-I) FUKASAWA N; (IKUM-I) IKUMO M; (KAWA-I) KAWAHARA T; (NAGA-I) NAGASHIGE K
CYC 4

PI	US 2001023981	A1 20010927 (200216)*	23	H01L021-44	
	JP 2001267350	A 20010928 (200216)	12	H01L021-60	<--
	KR 2001089139	A 20010929 (200220)		H01L023-12	
	US 6437432	**B1 20020820 (200257)**		**H01L023-52**	<--
	TW 484204	A 20020421 (200314)		H01L021-768	

ADT US 2001023981 A1 US 2000-745742 20001226; JP 2001267350 A JP 2000-78935 20000321; KR 2001089139 A KR 2001-3171 20010119; US 6437432 B1 US 2000-745742 20001226; TW 484204 A TW 2001-100287 20010105
PRAI JP 2000-78935 20000321
IC ICM H01L021-44; **H01L021-60**; H01L021-768; H01L023-12; **H01L023-52**
ICS H01L021-3205; H01L021-48; H01L021-50; **H01L021-56**; H01L023-02

AB US2001023981 A UPAB: 20020308
NOVELTY - A semiconductor device comprises a semiconductor substrate including signal pads and ground pads; an insulating film formed on the substrate; a **conductive** metal **film** formed on the insulating film and electrically connected to the ground pads; and first **interconnection** lines electrically connected to the signal pads and insulated from the **conductive** metal **film**.
DETAILED DESCRIPTION - A semiconductor device comprises a semiconductor substrate (21) including signal pads (25) and ground pads (26); an insulating film formed on the substrate; a **conductive** metal **film** (29A) formed on the insulating film and electrically connected to the ground pads; and first **interconnection** lines (28A) electrically connected to the signal pads and insulated from the **conductive** metal **film**. The **conductive** metal **film** is formed over a region including the first **interconnection** lines in a plan view of the device.
An INDEPENDENT CLAIM is also included for a method of producing the semiconductive device, comprising:
(a) forming a first insulating film on the substrate including the signal and ground pads except for positions where the signal and ground pads are formed;
(b) forming the **conductive** metal **film** on the first insulating film except for the positions where the signal pads are formed;
(c) forming a second insulating **film** over the **conductive** metal **film**;
(d) forming the **interconnection** lines on the second insulating film;
(e) forming **protrusion electrodes** each having a predetermined height on the **interconnection** lines; and

(f) providing **resin** sealing on the first and second insulating **films** (30, 31), the **conductive** metal **film**, the **interconnection** lines, and **sides** of the **protrusion electrodes**.

USE - As a semiconductor device.

ADVANTAGE - The inventive device has improved electrical characteristic to become a fast semiconductor device employing a high frequency. Since, the **conductive** metal **film** is electrically insulated from the **interconnection** lines, the **conductive** metal **film** does not cause a short circuit between the **interconnection** lines and the ground.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of a semiconductor device.

Substrate 21

First **protrusion electrodes** 22

Second **protrusion electrodes** 23 Sealing **resin** 24

Signal pads 25

Ground pads 26

First **interconnection** lines 28A

Conductive metal **film** 29A

First and second insulating films 30, 31 Dwg.3/14

TECH US 2001023981 A1UPTX: 20020308

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: The device includes first **protrusion electrodes** (22) electrically connected to the first **interconnection lines**; second **protrusion electrodes** (23) electrically connected to and formed directly on the **conductive** metal **film**; and a sealing **resin** (24) sealing the signal and ground pads, the insulating **film**, the **conductive** metal **film**, the first **interconnection** lines, and side of the first and second **protrusion electrodes**. The ground **pads** are connected directly to the **conductive** metal **film**. Protective metal films are formed on the signal or ground pads. The first **interconnection** lines are formed above the **conductive** metal **film**. Second **interconnection** lines electrically connect the ground **pads** and the second **protrusion electrodes**, and are included in the region. They are formed above the **conductive** metal **film**.

L41 ANSWER 17 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN
AN 2001-610477 [70] WPIX Full-text
DNN N2001-455666 DNC C2001-182282
TI Capacitor electrode used in semiconductor devices such as DRAM bit cells has dielectric post **protruding** dielectric **film**, a first **conductive film** on the dielectric post, and a second **conductive film** under the dielectric post.
DC L03 U12 U13 U14 V01
IN JIANG, B; MELNICK, B M; ROBERTS, D R; WHITE, B E
PA (MOTI) MOTOROLA INC
CYC 1
PI US 6274899 B1 20010814 (200170)* 12 H01L027-108
ADT US 6274899 B1 US 2000-574952 20000519
PRAI US 2000-574952 20000519
IC ICM H01L027-108
ICS H01G004-10; H01L027-112; H01L029-92
AB US 6274899 B UPAB: 20011129
NOVELTY - Capacitor **electrode** comprises: a dielectric **film** having a recess overlying a semiconductor device, a dielectric post protruding from the dielectric film and having an outer peripheral boundary defined by side walls, and a top surface; a first **conductive film** on the dielectric post, at least along its sidewalls; and a second **conductive film** under the dielectric post.

DETAILED DESCRIPTION - Preferred Features: The second **conductive film** lines the recess, and portions of the dielectric post, extend into the recess. The first and second **conductive films** are electrically connected together and define portions of a capacitor electrode. At least one of the **conductive films** includes a material selected from iridium, platinum, palladium, ruthenium, rhenium, rhodium and osmium.

A third **conductive film** can be formed over the top surface of the dielectric post, the first, second and third **conductive films** being electrically **interconnected** and defining portions of the capacitor electrode.

The portions of the dielectric post extending into the recess comprise an oxygen barrier.

An oxygen barrier including a material selected from iridium and ruthenium is disposed within the recess.

The oxygen barrier comprises:

(i) a **conductive layer** that lines the recess, and which is selected from iridium oxide, ruthenium oxide, titanium nitride, titanium aluminum nitride, titanium silicon nitride, tantalum nitride, tantalum aluminum nitride, tantalum silicon nitride, metal nitrides, metal borides and metal carbides; and

(ii) a dielectric material.

An INDEPENDENT CLAIM is given for an alternative embodiment of a capacitor electrode.

USE - Manufacture of semiconductor devices, especially dynamic random access memory (DRAM) bit cells.

ADVANTAGE - Thinner conductive materials can be used to form electrodes having larger overall surface area and are intrinsically easier to etch. The etch to define the capacitor electrode does not require patterning; instead, feature size and spacing is determined by patterning and etching of the dielectric posts. The cost of forming the electrode is reduced.

DESCRIPTION OF DRAWING(S) - The drawing shows an illustration of a cross-sectional view of a capacitor structure according to an embodiment of the invention.

Semiconductor device substrate 10
Field isolation regions 102
Doped regions 104
Gate dielectric film 106
Gate electrode 108
Dielectric film 110
Contact opening 112
Conductive fill material 116
Transistor 118
Conductive films 1004,1008, 1102
Bottom electrode of capacitor 1200 Dwg.12/18

L41 ANSWER 18 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN
AN 2001-448075 [48] WPIX Full-text
DNN N2001-331720

TI Solar battery has insulating substrate with hemispherical protrusions on which two **electrode layers** sandwiching P and N type semiconductor layers are formed.
DC U12
IN FUKUI, A; KIMOTO, K
PA (MIHI) MITSUI HIGH TEC KK; (MIHI) MITSUI HIGH TEC INC
CYC 2
PI JP 2001156316 A 20010608 (200148)* 7 H01L031-04
US 6420644 B1 20020716 (200248) H01L031-042
ADT JP 2001156316 A JP 1999-336789 19991126; US 6420644 B1 US 2000-723042 20001127
PRAI JP 1999-336789 19991126
IC ICM H01L031-04; H01L031-042
ICS H01L031-048
AB JP2001156316 A UPAB: 20010829
NOVELTY - An insulating substrate (1) has hemispherical protrusions on its surface. An **electrode layer** (10), P and N type amorphous silicon layers (11,12), and another **electrode layer** (13) consisting of transparent material, are formed sequentially on the substrate.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for solar battery manufacturing method.
USE - Solar battery.
ADVANTAGE - Uses heat resistant glass or **resin** as substrate so that manufacture of solar battery becomes simple. Secures large element area and stable output characteristics.
DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of solar battery.
Insulating substrate 1
Electrode layers 10,13
P and N type amorphous silicon layers 11,12 Dwg.2/10

L41 ANSWER 19 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN
AN 2000-278886 [24] WPIX Full-text
CR 1998-548150 [47]; 1999-606634 [52]; 2000-278885 [24]; 2000-669049 [65]
DNN N2000-210229
TI Variable resistor for high voltage applications, has connection terminal with cylindrical portion whose edge part protrudes from **insulated resin layer**, by connecting **conducting** rubber at **backside** of circuit board.
DC V01
PA (HOKU-N) HOKURIKU DENKI KOGYO KK
CYC 1
PI JP 2000077217 A 20000314 (200024)* 7 H01C013-00
JP 3187395 B2 20010711 (200140) 7 H01C013-00
ADT JP 2000077217 A Div ex JP 1998-62758 19860528, JP 1999-204651 19860528; JP 3187395 B2 Div ex JP 1998-62758 19860528, JP 1999-204651 19860528
FDT JP 3187395 B2 Previous Publ. JP 2000077217
PRAI JP 1998-62758 19860528; JP 1999-204651 19860528
IC ICM H01C013-00
ICS H01C001-02; H01C001-14
AB JP2000077217 A UPAB: 20010719
NOVELTY - Opening in insulated case (1) is filled with **insulated resin**, so that an **insulated resin** layer (6) is formed on backside of circuit board (5). Edge of cylindrical portion (7b) of a connection terminal (7) protrudes from the **insulated resin layer** by connecting cylindrical **conducting** rubber (7c) at **backside** of circuit board. A lead wire support (4) supports lead wire for focus output inside the case.
DETAILED DESCRIPTION - A sluder is provided between the insulated case (1) and the surface of circuit board (5). The circuit board having a resistor circuit pattern with variable resistance body is contained inside the insulated case.
USE - The variable resistor combined with fly back transformer is used for high voltage application such as in television receiver.
ADVANTAGE - The connection of variable resistor with fly back transformer can be performed simply and reliably, without connecting lead wire during final processing.
DESCRIPTION OF DRAWING(S) - The figure shows fragmentary sectional view of variable resistor.
Insulated case 1
Lead wire support 4
Circuit board 5
Insulated resin layer 6
Connection terminal 7

Cylindrical portion 7b
Cylindrical conducting rubber 7c Dwg.1/10

L41 ANSWER 20 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN
AN 2000-278885 [24] WPIX Full-text
CR 1998-548150 [47]; 1999-606634 [52]; 2000-278886 [24]; 2000-669049 [65]
DNN N2000-210228
TI High voltage variable resistor for use in television, has terminal provided at back side of circuit board, so that **conducting** rubber **protruding** from **resin** layer is inserted into cylindrical.
DC V01 V04
PA (HOKU-N) HOKURIKU DENKI KOGYO KK
CYC 1
PI JP 2000077216 A 20000314 (200024)* 7 H01C013-00
JP 3187394 B2 20010711 (200140) 7 H01C013-00
ADT JP 2000077216 A Div ex JP 1998-62758 19860528, JP 1999-204646 19860528; JP 3187394 B2 Div ex JP 1998-62758 19860528, JP 1999-204646 19860528
FDT JP 3187394 B2 Previous Publ. JP 2000077216
PRAI JP 1998-62758 19860528; JP 1999-204646 19860528
IC ICM H01C013-00
ICS H01C001-02; H01C001-14; H01R011-01
AB JP2000077216 A UPAB: 20010719
NOVELTY - A circuit board (5) with variable resistor circuit pattern, is provided inside an insulated case (1) having aperture at one end. The opening is filled with **resin** and an **insulated resin** layer (6) is provided to back side of circuit board. A connection terminal (7) at back side of circuit board has cylindrical portion (7b) to insert cylindrical **conducting** rubber (7c) **protruded** from the **resin** layer.
DETAILED DESCRIPTION - The terminal is provided such that the circular end of rubber is exposed from the edge of the cylindrical portion. A slider is provided between the insulated case and circuit board.
USE - For flyback transformer used in television .
ADVANTAGE - Since the conducting rubber is inserted into the cylindrical portion, need for fixing the conductor to flyback transformer side is avoided. The conducting rubber prevents reduction of dielectric strength.
DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of high voltage variable resistor.
Insulated case 1
Circuit board 5
Insulated resin layer 6
Connection terminal 7
Cylindrical portion 7b
Cylindrical conducting rubber 7c Dwg.1/10

L41 ANSWER 21 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN
AN 2000-226863 [20] WPIX Full-text
DNN N2000-170097 DNC C2000-069514
TI Multilayered anisotropic **conductivity film** for connecting LCDs and flexible board - has insulating layer and particle **layer** dispersed with electrically **conductive** particles and has thickness of particle layer below projection point of ball **bump**.
DC A85 L03 P81 U14 V04
PA (MATU) MATSUSHITA DENKI SANGYO KK
CYC 1
PI JP 11326935 A 19991126 (200020)* 7 G02F001-1345
JP 3438583 B2 20030818 (200356) 6 G02F001-1345
ADT JP 11326935 A JP 1998-125709 19980508; JP 3438583 B2 JP 1998-125709 19980508
FDT JP 3438583 B2 Previous Publ. JP 11326935
PRAI JP 1998-125709 19980508
IC ICM G02F001-1345
ICS H05K003-36

AB JP 11326935 A UPAB: 20000502
NOVELTY - The particle layer (4) is distributed with electrically conductive particles (5). The anisotropic **conductivity film** (20) is formed by laminating insulating layer (3) and particle layer (4), mechanically. The thickness of the particle layer (4) is made below the projection of the point of the ball **bump** (2).
DETAILED DESCRIPTION - Ball **bump** (2) with a two step **protrusion** is formed on semiconductor chip (1). The insulating layer (3) is formed by an **insulating** and adhesive **resin** . An INDEPENDENT CLAIM is also included for connecting method of LCD and flexible board.
USE - For connecting LCDs with flexible board. Also for connecting semiconductor chip onto printed wiring board.
ADVANTAGE - The junction reliability is increased using simple technique.
DESCRIPTION OF DRAWING - The figure shows the sectional view of the multilayered anisotropic **conductivity film**. (1) Semiconductor chip; (2) Ball **bump**; (3) Insulating layer; (4) Particle **layer**; (5) Electrically **conductive** particle; (20) Anisotropic **conductive film**. Dwg.1/8
FS CPI EPI GMPI
FA AB; GI
MC CPI: A12-E07A; A12-E07C; A12-L03B; L03-G05A; L03-H04E; L04-C10; L04-C17
EPI: U14-K01A4B; V04-R04

L41 ANSWER 22 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN
AN 1999-625309 [54] WPIX Full-text
DNN N1999-462050 DNC C1999-182637
TI Chip mounting method for manufacturing semiconductor device - involves connecting electrically metal bump and electrode of chip and circuit board respectively by thermocompression bonding process using alloy layer.
DC A85 L03 U11
PA (MATE) MATSUSHITA ELECTRONICS CORP
CYC 1
PI JP 11274241 A 19991008 (199954)* 12 H01L021-60
ADT JP 11274241 A JP 1998-79632 19980326
PRAI JP 1998-79632 19980326
IC ICM H01L021-60
AB JP 11274241 A UPAB: 20000105
NOVELTY - A bonding tool (30) **couples** a metal **bump** (27) of a semiconductor chip (10), to an electrode (41) of a circuit board (40) by thermocompression bonding process through an alloy layer. A **resin** layer (24B) that surrounds the metal bump is stiffened, thereby promoting coupling between the chip and the circuit board.
DETAILED DESCRIPTION - **Protruding electrodes** (23) are formed on each of the pads (21) of a wafer (20). A **resin** layer (24A) surmounts the substrates including the **electrodes** (23). The **resin layer** is then polished along with the electrode, so that surface of the electrode is in agreement with that of the **resin** layer (24b). Multiple chips (10) are produced by slicing the substrate suitably.
USE - For manufacturing semiconductor devices.
ADVANTAGE - Since chip is mounted on circuit board, bare chip mounting process becomes possible. Therefore manufacturing cost is reduced. Electrical connection between electrode and bump and between circuit board and chip are performed simultaneously using alloy layer and **resin** layer. Thus product yield is improved.
DESCRIPTION OF DRAWING - The figure shows sectional view of process involved in manufacturing of semiconductor device. (10) Multiple chips; (20) Wafer; (21) Pads; (23,41) Electrodes; (24A,24B,24b) **Resin** layers; (30) Bonding tool; (40) Circuit board. Dwg.1/12

L41 ANSWER 23 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN
AN 1999-173068 [15] WPIX Full-text
DNN N1999-127087
TI Semiconductor device mounting method on wiring board - involves filling gap between semiconductor device and wiring board using combination of electroconductive glue and **resin layer** or anisotropic electrically **conductive** sheet.
DC U11 V04
IN BESSHO, Y; HASE, N; ITAGAKI, M; NAKAMURA, Y; TAKEZAWA, H; YUHAKU, S
PA (MATU) MATSUSHITA DENKI SANGYO KK; (MATU) MATSUSHITA ELECTRIC IND CO LTD

CYC 2
PI JP 11026631 A 19990129 (199915)* 6 H01L023-12
US 6207550 B1 20010327 (200119) H01L021-44
ADT JP 11026631 A JP 1997-176844 19970702; US 6207550 B1 US 1998-107319 19980630
PRAI JP 1997-176844 19970702
IC ICM H01L021-44; H01L023-12
ICS H05K001-18
AB JP 11026631 A UPAB: 19990416
NOVELTY - A multilayered wiring board has **several protruding electrodes** (1) on its surface. An electrode (8) of semiconductor device and the **protruding electrodes** are electrically bonded using an electroconductive glue (6). The semiconductor device (7) is mounted on wiring board and gap between them is filled using a combination of electroconductive glue and sealing **resin** (9) or an anisotropic electrically- conductive sheet.
USE - None given.
ADVANTAGE - Offers reliable semiconductor mounting without requiring severe flat property of wiring board. The possibility of physical destruction by connection is reduced hence the reliability of electric connection can be improved. Stress generated in the semiconductor device or wiring board is dispersed. The dynamic damage to semiconductor device and wiring board is reduced. DESCRIPTION OF DRAWING(S) - The figure shows the mounting method of semiconductor device using electroconductive view and sealing **resin**. (1) **Protruding electrodes** ; (6) Electroconductive glue; (7) Semiconductor device; (8) Semiconductor device electrode; (9) Sealing **resin**. Dwg.1/3

L41 ANSWER 24 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN
AN 1999-159570 [14] WPIX Full-text
DNN N1999-116167
TI **Resin** sealed package for semiconductor device - includes stud **bump** which contacts metal **film** formed on semiconductor device.
DC U11
PA (FUIT) FUJITSU LTD
CYC 1
PI JP 11017054 A 19990122 (199914)* 15 H01L023-12
JP 3181243 B2 20010703 (200139) 15 H01L023-12
ADT JP 11017054 A JP 1997-168578 19970625; JP 3181243 B2 JP 1997-168578 19970625
FDT JP 3181243 B2 Previous Publ. JP 11017054
PRAI JP 1997-168578 19970625
IC ICM H01L023-12
ICS **H01L021-60; H01L023-28;** H01L023-50
AB JP 11017054 A UPAB: 19990412
NOVELTY - The semiconductor device (11) is sealed by a **resin** package (12). A **resin** protrusion (17) is formed on the mounting **side** of the **resin** package. The **resin protrusion contacts** a **metal film** (13) formed on the semiconductor device. A wire (18) connects the electrode pad (14) and the metal **film**. A stud **bump** (40) is provided in the metal **film** such that it pierces into the interior of the package.
USE - For semiconductor device.
ADVANTAGE - The peeling of **metal film** from **resin protrusion** is prevented. DESCRIPTION OF DRAWING(S) - The drawing shows the sectional view of the semiconductor device. (11) Semiconductor device; (12) **Resin** package(13) Metal **film** ; (14) **Electrode pad**; (17) **Resin protrusion**; (18) Wire; (40) Stud **bump**. Dwg.1/25

L41 ANSWER 25 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN
AN 1995-095274 [13] WPIX Full-text
DNN N1995-075069 DNC C1995-043736
TI Layer type inductor - incorporates coil electric **conductor** having protrusions and **coated** with **insulated** **resin** or impregnated with **insulating** varnish.
DC A85 L03 V02
PA (TOHM) TOKIN CORP
CYC 1
PI JP 07022252 A 19950124 (199513)* 4 H01F027-32
ADT JP 07022252 A JP 1993-189429 19930630
PRAI JP 1993-189429 19930630
IC ICM H01F027-32
ICS H01F027-28
AB JP 07022252 A UPAB: 19950404
The layer type inductor consists of flat board type coil electric conductors (2). On the surface of the electric conductors, an electric insulation skin layer (3) is formed. The different **layers** of electric **conductor** have mutual connections. A **protruding line** (5) of the secondary side coil (2b), is formed on the electric conductor so that, it does not overlap with the **protruding line** (4) of the primary side coil (2a). The moulding of the electric conductor is done by **insulated** **resin** or impregnation process of **insulating resin** in it.
USE/ADVANTAGE - For use in winding wire electric conductor. Guarantees electric insulation breakdown voltage characteristics between coil electric conductors. Enables automatic assembly. Dwg.2/5

L41 ANSWER 26 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN
AN 1994-318665 [40] WPIX Full-text
DNN N1994-261841 DNC C1994-151778
TI **Interconnector** for effectively connecting electronic devices and circuits vertically through multilayer circuit boards - comprising preformed conductive cones which are forced through **resin** supporting member under pressure to make contact with wiring patterns formed by etching foil on opposite sides.
DC A85 L03 U11 U14 V04
IN ARAI, Y; IKEGAYA, F; IMAMURA, E; KOWATARI, S; MORI, T; ODAIRO, H; SASAOKA, K; WADA, Y; ODAIRA, H
PA (TOKE) TOSHIBA KK
CYC 8
PI EP 620701 A2 19941019 (199440)* EN 30 H05K003-40
R: DE FR GB
JP 06342977 A 19941213 (199509) 9 H05K003-40
EP 620701 A3 19950215 (199540) H05K003-40
US 5600103 A 19970204 (199711) 22 H05K001-00
EP 620701 B1 19980708 (199831) EN H05K003-40
US 5822850 A 19981020 (199849) H05K003-02
PRAI JP 1993-90177 19930416; JP 1993-131726 19930602;
JP 1993-152006 19930623; JP 1993-223329 19930908
REP No-SR.Pub; DE 9102817; US 3488429; US 3835531; US 4991285
IC ICM H01R011-01; H05K001-00; H05K001-11; H05K003-02; H05K003-40; H05K003-46
ICS **H05K001-18; H05K003-32**
AB EP 620701 A UPAB: 19941212
Interconnector (1) comprises synthetic **resin** supporting member (4) having nearly circular, cone shaped conductive lead portions (2') pierced vertically into it at spaced locations. The bottom surface of each lead portion is fully exposed on one main surface of the **resin** supporting member and the top surface of each protrudes from the other surface. Also claimed is a printed wiring board having an **insulating** synthetic **resin** supporting member pierced by conductive lead portions at intervals and a metal wiring pattern connected to at least one of the conductive lead portions. Also claimed is a method of fabricating the printed wiring board by superposing a main surface of the synthetic **resin** sheet on a main surface of a supporting member with conductive bumps at predetermined positions and pressurizing the laminate thus formed so that the bumps pierce vertically into the **resin** sheet to form through-type conductive lead portions.

USE - **Interconnector** effectively connects electronic devices and forms electronic circuits on printed wiring boards having densely connected lines and components.

ADVANTAGE - The conductive bumps can be precisely and densely formed and located using a printing or plating method and can be reliably connected to an opposed **conductive layer**. Consequently, circuit boards can be fabricated with high efficiency with few rejects. (Reissued from week 9440 to add EPI classifications/ Reprinted in week 9442)

Dwg.1/17

ABEQ US 5600103 A UPAB: 19970313

An inter-connector, comprising: a synthetic **resin** supporting member; and nearly circular cone shaped conductive lead portions pierced vertically into the synthetic **resin** supporting member and spaced apart from each other, where a bottom surface of each of the circular cone shaped conductive lead portions is flatly exposed on one main surface of the synthetic **resin** supporting member and top portions of the circular cone shaped **conductive** lead portions **protrude** from **other** surface of the synthetic **resin** supporting member.

Dwg.1/29

L41 ANSWER 27 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN

AN 1993-243453 [30] WPIX Full-text

DNN N1993-187266

TI Flexible circuit wiring board with finger lead conductors - has insulating base with conductor pattern covered by protection layer with notches for formation of conductors by abrasion while radiating by excimer laser.

DC U11

IN INABA, M; IWAYAMA, T; MIYAGAWA, A

PA (NIMF) NIPPON MEKTRON KK

CYC 3

PI	WO 9314516 W: DE US	A1	19930722 (199330)*	JA 10	H01L021-60	<--
	JP 05190755	A	19930730 (199335)		H01L023-50	
	US 5444188	**A**	**19950822 (199539)**	**5**	**H05K003-00**	
	US 5446245	**A**	**19950829 (199540)**	**6**	**H05K001-02**	
	JP 3088175	B2	20000918 (200048)	4	H01L021-60	<--

ADT WO 9314516 A1 WO 1993-JP28 19930112; JP 05190755 A JP 1992-24469 19920114; US 5444188 A WO 1993-JP28 19930112, US 1993-117010 19930908; US 5446245 A Div ex US 1993-117010 19930908, US 1994-251388 19940531; JP 3088175 B2 JP 1992-24469 19920114

FDT US 5444188 A Based on WO 9314516; JP 3088175 B2 Previous Publ. JP 05190755

PRAI JP 1992-24469 19920114

REP JP 03096245; JP 61137353

IC ICM **H01L021-60**; H01L023-50; H05K001-02

ICS H05K003-40

AB WO 9314516 A UPAB: 19951019

The flexible circuit wiring board has circuit wiring conductors (2A), each having a flexible **insulation resin** layer whose width is nearly equal to that of the circuit wiring conductor (2A), on a part of at least one **side** of the **conductor** (2A), forming a part (6) for reinforcing a terminal.

On one side of an insulation base material (1) a required circuit wiring conductor pattern (2) is formed. On the top surface of the pattern (2), a surface protection layer (5) is formed in which notch parts (7) are provided at places where the circuit wiring conductors (2A) are to be formed. A part of the insulation base material (1) is removed at the places where the circuit wiring conductors (2A) are to be formed, by abrasion while projecting an excimer laser beam onto it from the insulating base material (1) side.

ADVANTAGE - Structure is hard to deform even with fine circuit wiring **conductors protruded** in form of finger leads.

ADVANTAGE - Structure is hard to deform even with fine circuit wiring **conductors protruded** in form of finger leads. Dwg.2/4

Dwg.2/4

ABEQ US 5444188 A UPAB: 19951004

flexible circuit wiring board having protruding, closely spaced leads, which are intended to be attached to a circuit device, is fabricated by forming a conductor pattern on a first surface of an insulating substrate, adhering a protection **layer** to the **conductor** pattern and employing a laser to selectively etch away the substrate.

The etching process leaves a reinforcing coating of the protective layer on the leads at least in the portions thereof which lie at the boundary of the area from which the substrate has been removed.

The method of producing flexible circuit wiring boards involves forming a circuit wiring pattern consisting of number conductors on one surface of an insulating base member. A surface protection layer is adhered to the exposed surface of the circuit wiring pattern, and has at least a first cutaway portion at a location where conductors of the wiring pattern are to be terminated as projecting finger-like leads.

The insulating base member is removed from areas where the leads are to be formed by projecting the beam of an excimer laser onto the base member. The cut-away portion of the surface protection layer is formed by projecting the excimer laser beam onto the exposed surface of the protection layer to remove a portion of the layer.

ADVANTAGE - Increased wiring density.

Dwg.1,2/4

ABEQ US 5446245 A UPAB: 19951011

The printed circuit comprises a flexible insulating base member having at least a first edge which at least in part defines a connection region and an aperture in the base member. A pattern of conductors are supported on the base member, at least some of which extend outwardly from the base member beyond the first edge into the connection region.

A flexible protective **layer** of non-**conductive** material is formed over the pattern of conductors on the base member, portions of which extend beyond the base member first edge in registration with the outwardly extending conductors to enhance the structural integrity of the conductors in the connection region. The protective layer comprises an insulating film and an adhesive, the adhesive securing the **film** to the **conductors**.

L41 ANSWER 28 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN

AN 1993-122913 [15] WPIX Full-text

DNN N1993-093693 DNC C1993-055043

TI Forming **protruded electrode** of semiconductor device - by applying 1st and 2nd metal films, then simultaneously depositing metal coated soft balls and electroplating film.

DC L03 M11

PA (OKID) OKI ELECTRIC IND CO LTD

CYC 1

PI JP 05062981 A 19930312 (199315)* 7 H01L021-321

ADT JP 05062981 A JP 1991-283378 19911030

PRAI JP 1991-145075 19910618

IC ICM H01L021-321

ICS C23C018-31; C25D005-02; C25D015-02; **H01L021-60**

AB JP 05062981 A UPAB: 19930924

The formation comprises (a) forming a first metallic film to at least ensure close attaching and preventing metal diffusion, and a second metallic film to improve attachability of electroplating in the post-process and stabilising chemically, on the electrode of the semiconductor device, and (b) forming the **protruded electrode** consisting of one **layer** or arrayed soft balls on the second metallic film by suspending metal coated soft balls in electroplating bath, and depositing the plating metal and the balls together.

Pref. the ball is plastic and coated with Ni, Au, Cu, Co, Sn, Ag, Pd, Pt, Ph and Ru, non-electrolytically.

USE/ADVANTAGE - Used for formation of the **protruded electrode** of the semiconductor device to be used for the chip-on-glass mounting or the chip-on-board mounting. Good connection of the electrode can be obtd. even with small loading. Damage on the device and the electrode pad can be reduced. 1/8

FS CPI

FA AB; GI

L41 ANSWER 29 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN
AN 1992-303901 [37] WPIX Full-text
DNN N1992-232706 DNC C1992-135045
TI Simply prepared lightweight LC panel having improved contrast - has insulator protrusions formed on signal lines of array substrate, polymer dispersed LC filled in between protrusions and transparent **electrode layer** formed on LC.
DC A85 L03 P81 U14
PA (MATU) MATSUSHITA ELEC IND CO LTD
CYC 1
PI JP 04208924 A 19920730 (199237)* 10 G02F001-1333
ADT JP 04208924 A JP 1990-317222 19901120
PRAI JP 1990-317222 19901120
IC ICM G02F001-1333
ICS G02F001-335
AB JP 04208924 A UPAB: 19931006
The panel comprises insulator protrudings formed on signal lines of an array substrate, a polymer dispersed LC filled in between the protrudings, and an **electrode layer** of a transparent electric conductor formed on LC.

Pref an optical mask layer is formed on the protrudings; the protrudings are formed on the signal line as stripes; and no substrate is placed on the **electrode layer**. Pref. the protrudings are formed on the signal line of the substrate, a **resin** containing LC is coated on it, a separable **resin** film is laminated on it, the **resin** is flatted by pressing, the **resin** is cured, then the film is removed.

USE/ADVANTAGE - The panel is suitable for TV, the method allows production of lightweight and high contrast LC panel.

In an example, LC was prepared from a source drive IC (12), gate drive IC (13), ITO opposed electrode (14), SiNx insulating protection film (15), wiring (19) for impressing required potential to (14), conductor paste (17) for connecting (14) and (19), LC polymer (18, 21) (e.g. nematic LC), source signal line (22). Picture element electrode (23) connected to TFT and insulator protrudings (25) formed on (22) were formed on array substrate (11) by conventional method using photolithography etc. (Dwg.1a,b/1a,b/9

L41 ANSWER 30 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN
AN 1992-246802 [30] WPIX Full-text
TI Aperture formation method on **metal protrusion** substrate - forming **conductive film** on insulated substrate, insulation **film** on **conductive film** and mask for photoresist etching on insulation film NoAbstract.
DC U11
PA (MATU) MATSUSHITA ELEC IND CO LTD
PI JP 04167536 A 19920615 (199230)* 5 H01L021-60 <--
ADT JP 04167536 A JP 1990-295772 19901031
PRAI JP 1990-295772 19901031
IC ICM **H01L021-60**

L41 ANSWER 31 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN
AN 1992-220693 [27] WPIX Full-text
TI Substrate with **metal protrusion** for mounting IC - has **conductive film**, rectangular or circular opening, and **metal protrusion**, thus reduces damage to chip NoAbstract.
PA (MATU) MATSUSHITA ELEC IND CO LTD
PI JP 04082226 A 19920316 (199227)* 5 H01L021-321
PRAI JP 1990-196635 19900724
IC ICM H01L021-321
ICS **H01L021-60**

L41 ANSWER 32 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN

AN 1992-076005 [10] WPIX Full-text

TI Electrical connecting member for fixing circuit parts on substrate - comprises holder of insulative material in which are embedded **conductive** members, with ends **protruding** and covered with **conductive** adhesive **layer** of pulverised metal or metallised ceramic powder.

DC U11 U14 V04

IN KADOKURA, S; YOSHIZAWA, T

PA (CANO) CANON KK

CYC 2

PI JP 04019972 A 19920123 (199210)* 6
US 5174766 A 19921229 (199303)B 16 H01R013-00

ADT JP 04019972 A JP 1990-121496 19900511; US 5174766 A Cont of US 1991-697776 19910509, US 1991-810444 19911219

FDT US 5174766 A JP 04019971, JP 04019972

PRAI JP 1990-121496 19900511; JP 1990-121494 19900511; JP 1990-121495 19900511

IC ICM H01R013-00
ICS **H01L021-60**; H01R004-04; H01R009-09; H01R011-01; **H05K001-18**; H05K003-36

AB JP 04019972 A UPAB: 19990922
The electrical connecting member includes a holder made of electrically insulative material, and a number of conductive members electrically insulated from each other and embedded in the holder and having ends exposed from the holder. A **conductive** adhesive **layer** eutectoidally formed by electrophoresis from an adhesive **resin** solution including one or both of pulverised metal powder and metallised ceramic powder is disposed on the end of each conductive member exposed from one holder surface.

The **conductive** adhesive **layers** and the **other** ends of the **conductive** members exposed from the **other** holder surface are flush with or protruded from the surfaces of the holder. Wirings in or on the holder surface connect some conductive members together.

ADVANTAGE - Easily **interconnects** circuit parts with low temps. by using connecting member with **conductive** adhesive **layer** on connecting portions. (First major country equivalent to JP4019970/1/2)

FS EPI

FA AB; GI

MC EPI: U11-D03A9; U11-E01X; U14-H03A2; V04-A09; V04-M05; V04-Q02B; V04-A06; V04-A07; V04-B01

L41 ANSWER 33 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN

AN 1992-076004 [10] WPIX Full-text

TI Electrical connecting member for fixing circuit parts on substrate - comprises holder of insulative material in which are embedded **conductive** members, with ends **protruding** and covered with **conductive** adhesive **layer** of pulverised metal or metallised ceramic powder.

DC U11 U14 V04

IN KADOKURA, S; YOSHIZAWA, T

PA (CANO) CANON KK

CYC 2

PI JP 04019971 A 19920123 (199210)* 6
US 5174766 A 19921229 (199303)B 16 H01R013-00

ADT JP 04019971 A JP 1990-121495 19900511; US 5174766 A Cont of US 1991-697776 19910509, US 1991-810444 19911219

FDT US 5174766 A JP 04019971, JP 04019972

PRAI JP 1990-121495 19900511; JP 1990-121494 19900511;
JP 1990-121496 19900511

IC ICM H01R013-00
ICS **H01L021-60**; H01R004-04; H01R009-09; H01R011-01; **H05K001-18**; H05K003-36

AB JP 04019971 A UPAB: 19990922
The electrical connecting member includes a holder made of electrically insulative material, and a number of conductive members electrically insulated from each other and embedded in the holder and having ends exposed from the holder. A **conductive** adhesive **layer** eutectoidally formed by electrophoresis from an adhesive **resin** solution including one or both of pulverised metal powder and metallised ceramic powder is disposed on the end of each conductive member exposed from one holder surface.

The **conductive** adhesive **layers** and the **other** ends of the **conductive** members exposed from the **other** holder surface are flush with or protruded from the surfaces of the holder. Wirings in or on the holder surface connect some conductive members together.

ADVANTAGE - Easily **interconnects** circuit parts with low temps. by using connecting member with **conductive** adhesive **layer** on connecting portions. (First major country equivalent to JP4019970/1/2)

L41 ANSWER 34 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN
AN 1992-076003 [10] WPIX Full-text
TI Electrical connecting member for fixing circuit parts on substrate - comprises holder of insulative material in which are embedded **conductive** members, with ends **protruding** and covered with **conductive** adhesive **layer** of pulverised metal or metallised ceramic powder.
DC U11 U14 V04
IN KADOKURA, S; YOSHIZAWA, T
PA (CANO) CANON KK
CYC 2
PI JP 04019970 A 19920123 (199210)* 6
US 5174766 A 19921229 (199303)B 16 H01R013-00
ADT JP 04019970 A JP 1990-121494 19900511; US 5174766 A Cont of US 1991-697776 19910509, US 1991-810444 19911219
FDT US 5174766 A JP 04019971, JP 04019972
PRAI JP 1990-121494 19900511; JP 1990-121495 19900511; JP 1990-121496 19900511
IC ICM H01R013-00
ICS **H01L021-60**; H01R004-04; H01R009-09; H01R011-01; **H05K001-18**; H05K003-36
AB JP 04019970 A UPAB: 19990922
The electrical connecting member includes a holder made of electrically insulative material, and a number of conductive members electrically insulated from each other and embedded in the holder and having ends exposed from the holder. A **conductive** adhesive **layer** eutectoidally formed by electrophoresis from an adhesive **resin** solution including one or both of pulverised metal powder and metallised ceramic powder is disposed on the end of each conductive member exposed from one holder surface.

The **conductive** adhesive **layers** and the **other** ends of the **conductive** members exposed from the **other** holder surface are flush with or protruded from the surfaces of the holder. Wirings in or on the holder surface connect some conductive members together.

ADVANTAGE - Easily **interconnects** circuit parts with low temps. by using connecting member with **conductive** adhesive **layer** on connecting portions. (First major country equivalent to JP4019970/1/2)

L41 ANSWER 35 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN
AN 1987-343440 [49] WPIX Full-text
DNN N1987-257151
TI Ultrasonic transducer for on-line applications - has nose piece contacting sheet material and attached to parallel piped-shaped piezoelectric element.
DC S02 V06
IN BOKOWSKI, G A; VAHEY, D W
PA (ACCU-N) ACCU RAY CORP; (ACCU-N) ACCURAY CORP; (PROC-N) PROCESS AUTOM BUSIN
CYC 7
PI EP 248512 A 19871209 (198749)* EN 17
R: DE FR GB IT SE
US 4713572 A 19871215 (198806) 7
CA 1287913 C 19910820 (199138)
EP 248512 B1 19920819 (199234) EN 9 G01H011-08
R: DE FR GB IT SE
DE 3781207 G 19920924 (199240) G01H011-08
ADT EP 248512 A EP 1987-303010 19870407; US 4713572 A US 1986-872049 19860606; EP 248512 B1 EP 1987-303010 19870407; DE 3781207 G DE 1987-3781207 19870407, EP 1987-303010 19870407
FDT DE 3781207 G Based on EP 248512
PRAI US 1986-872049 19860606
REP A3...8914; No-SR.Pub; US 3935484; US 3950660; US 4291577; US 4562372
IC ICM G01H011-08
ICS H01L041-08; H04R017-00
AB EP 248512 A UPAB: 19930922
The piezo-electric element (4), e.g. of a lead zirconate-lead titanate ceramic, has nominal dimensions of length (6) one inch, width (8) one fourth of an inch and a thickness (10) of one eighth of an inch. An electrode film is deposited on one surface (12) and an opposite main surface. A nose-piece is rigidly attached to the element by an adhesive, pref. a conductive epoxy.

Electrical contact between the electrode film and the external electrical communication system can be by a **protruding glob** of conductive epoxy. The sheet material is brought into contact with the transducer at the contacting surface of the nose-piece.

USE/ADVANTAGE - Withstands rigours of on-line environment while avoiding damage to sheet material due to movement. Detects ultrasonic waves of predominantly one propagation mode for measuring physical parameter of sheet material.

1/5

ABEQ DE 3781207 G UPAB: 19930922
The piezo-electric element (4), e.g. of a lead zirconate-lead titanate ceramic, has nominal dimensions of length (6) one inch, width (8) one fourth of an inch and a thickness (10) of one eighth of an inch. An electrode film is deposited on one surface (12) and an opposite main surface. A nose-piece is rigidly attached to the element by an adhesive, pref. a conductive epoxy.

Electrical contact between the electrode film and the external electrical communication system can be by a **protruding glob** of conductive epoxy. The sheet material is brought into contact with the transducer at the contacting surface of the nose-piece.

USE/ADVANTAGE - Withstands rigours of on-line environment while avoiding damage to sheet material due to movement. Detects ultrasonic waves of predominantly one propagation mode for measuring physical parameter of sheet material.

ABEQ EP 248512 B UPAB: 19930922
A transducer for transmitting ultrasound into a medium through which ultrasound is propagated or for receiving ultrasound therefrom, and comprising a piezoelectric element having opposite parallel faces one of which, in use, is presented toward said medium, and upon both of which faces respective electrode films are deposited, with a protective covering over the electrode film on said face that, in use, is presented toward said medium, characterised in that the piezoelectric element (4) has the shape of a parallelepiped whereof the length (6) is greater than the width (8) and the width is greater than the thickness (10), and the respective electrode films are deposited on opposite surfaces (12, 14) whose dimensions are the length and width of the element, the direction of vibration of the element when a voltage is applied across said electrode

lying along the longitudinal axis (x) of the element, and the protective covering comprises at least a nosepiece (16) having two opposite surfaces one of which (18) constitutes a joining surface that is rigidly affixed to one of said electrode surfaces of the piezoelectric element, and the other (20) being contacting surface for contact with said medium (22).
(Dwg.1,2,4
1,2,4/5

ABEQ US 4713572 A UPAB: 19930922
The transducer comprises a piezoelectric element having the shape of a parallelepiped, and a metallic nosepiece rigidly attached to a surface of the element and adapted for contact with sheet material through which ultrasound is propagated. The contacting surface is confined to a location that is near a longitudinal extreme of the transducer.

A portion of the nosepiece is rounded or bevelled with the contacting surface being rectangular or spherically convex.

ADVANTAGE - Provides efficient transmission of ultrasound and reduces risk of damage to moving sheet material.

L41 ANSWER 36 OF 36 WPIX COPYRIGHT THOMSON DERWENT on STN
AN 1986-228593 [35] WPIX Full-text
TI Mfg. substrate for forming **protruding metal** - forming **conductive film**, insulating **film** and resist pattern, first two having sequential holes NoAbstract DWg 2/2.
DC U11
PA (MATU) MATSUSHITA ELEC IND CO LTD
CYC 1
PI JP 61158166 A 19860717 (198635)* 6
ADT JP 61158166 A JP 1984-275494 19841229
PRAI JP 1984-275494 19841229
IC **H01L023-48**
FS EPI
FA NOAB
MC EPI: U11-D03A; U11-E01

L49 ANSWER 3 OF 10 EUROPATFULL COPYRIGHT WILA on STN

PATENT APPLICATION - PATENTANMELDUNG - DEMANDE DE BREVET

AN 1011141 EUROPATFULL ED 20000702 EW 200025 FS OS Full-text
TIEN Semiconductor device and process for producing it.
IN Kobayashi, Syoichi, Shinko Elec. Ind. Co. Ltd., Aza Shariden Oaza Kuri,
PA SHINKO ELECTRIC INDUSTRIES CO. LTD., 711, Aza Shariden, Oaza Kurita,
PI EP 1011141 A2 20000621
PRAI JP 1998-359229 19981217
ABEN A semiconductor device has excellent bonding strength of **bumps** (38) with their respective **protruded electrodes** (32) and has high reliability. A wiring pattern (28) to be connected to an electrode (22) of a semiconductor chip (20) is formed on an insulating film (23) formed on the semiconductor chip (20) in which the **electrode** (20) is formed. **Protruded electrodes** (32) are formed on the wiring pattern (28). The wiring pattern (28) is covered with a protective **film** (36), and a **bump** (38) for external connection is formed on the end portion of each of the **protruded electrodes** (32) exposed from the protective **film** (36). The **bump** (38) is formed in such a manner that the bump is bonded to at least the entire end face of each of the **protruded electrodes** (32). <image>

DETDEN
CLMEN. . . electrode of a semiconductor chip is formed on an insulating film formed on the semiconductor chip surface on which the **electrode** is formed, **protruded electrodes** are formed on the wiring pattern, the wiring pattern is covered with a protective film, and a bump for external connection is formed on the end portion of each of the **protruded electrodes** exposed from the protective film,

the bump being formed by bonding the bump to the at least entire end face of each of the **protruded electrodes**.

2. . . . device according to claim 1, wherein a barrier plated layer is formed on the end face of each of the **protruded electrodes**, and the **bump** is formed in such a manner that the bump is bonded to the entire barrier plated layer.

3. . . . in such a manner that the top surface of the protective film is lower than the position at which the **bump** is bonded to the **protruded electrode**.

4. . . . according to claim 1 or 2, wherein an oxide film is formed on the peripheral surface of each of the **protruded electrodes**, and there is a gap between the protective film and the peripheral surface of each of the **protruded electrodes**.

5. . . . in such a manner that the top surface of the protective film is higher than the position at which the **bump** is bonded to the **protruded electrode**, and that part of the peripheral surface of the bump is contacted with the protective film.

6. . . . electrode of a semiconductor chip is formed on an insulating film formed on the semiconductor chip surface on which the **electrode** is formed, **protruded electrodes** are formed on the wiring pattern, the wiring pattern is covered with a protective film, and a bump for external connection is formed on the end portion of each of the **protruded electrodes** exposed from the protective film, the process comprising the steps of:

covering the wiring pattern formed on the insulating. . . resist layer to expose part of the wiring pattern;

plating the wiring pattern within the holes to form the **protruded electrodes**;

removing the resist layer;

effecting sealing by supplying a **resin** to the wiring pattern to form a **resin** layer having a top surface lower than that of the **protruded electrodes**, thereby forming a protective film; and

forming the **bump** on each of the **protruded**

L49 ANSWER 4 OF 10 EUROPATFULL COPYRIGHT WILA on STN

PATENT APPLICATION - PATENTANMELDUNG - DEMANDE DE BREVET

AN 987749 EUROPATFULL ED 20000402 EW 200012 FS OS Full-text
TIEN Semiconductor device, electrode structure therefore, and production thereof.
TIDE Halbleitervorrichtung, Elektrodenstruktur fuer diesselbe und dessen Herstellungsverfahren.
TIFR Dispositif semiconducteur, sa structure d'electrode et son procede de fabrication.
IN Kirloskar, Mohan, c/o Shinko Electric America Inc., 3211 Scott Blvd, Suite 101, Santa Clara, California 95054, US;
Horiuchi, Michio, c/o Shinko Electric Ind. Co.Ltd., 711 Aza Shariden, Oaza Kurita, Nagano-shi, Nagano 380-0921, JP;
Takeuchi, Yukiharu, c/o Shinko Electric Ind.Co.Ltd, 711 Aza Shariden, Oaza Kurita, Nagano-shi, Nagano 380-0921, JP
PA SHINKO ELECTRIC INDUSTRIES CO. LTD., 711, Aza Shariden, Oaza Kurita, Nagano-shi, Nagano 380-0921, JP
PAN 1161831
AG Rackham, Stephen Neil, GILL JENNINGS & EVERY, Broadgate House, 7 Eldon Street, London EC2M 7LH, GB
PI EP 987749 A2 20000322
OD 20000322
AI EP 1999-306984 19990902
PRAI JP 1998-248146 19980902
ABEN A semiconductor device comprising a semiconductor chip (10) having an electrode terminal carrying surface and electrode terminals (12) formed on, and carried by, the electrode terminal carrying surface. Leads (30) extend substantially parallel to the electrode terminal carrying surface, each lead (30) having at least one curved portion, a first bump (40) and a second bump (28) which are formed on opposite ends respectively of each of the leads (30) and protrude from the ends in opposite directions toward and away from, respectively, the electrode terminal carrying surface. The electrode terminals (12) of the semiconductor chip (10) are each bonded to a **top** of the first **bump** (40) of the lead (30) to support the leads (30) at a distance from the electrode terminal carrying surface of the semiconductor chip (10). <image>

DETDEN. . . semiconductor wafer in which high precise positioning is necessary. A semiconductor water may not have a terminal on a passivation **film** and the **electrode** connection terminal 40 may be directly bonded to an electrode terminal of the chip precursors of the wafer.

CLMEN. . . extending substantially parallel to said one side of the card base and having at least one curved portion, said probe **contact** and said bond terminal **protruding** from one and the other ends of the lead, respectively, in opposite directions toward and away from said one side. . .

L49 ANSWER 5 OF 10 EUROPATFULL COPYRIGHT WILA on STN

PATENT APPLICATION - PATENTANMELDUNG - DEMANDE DE BREVET

AN 831525 EUROPATFULL ED 19980405 EW 199813 FS OS Full-text
TIEN Method for forming **protruding electrode**.
IN Shoji, Kazutaka, NEC Corporation, 7-1, Shiba 5-chome, Minato-ku, Tokyo,
PA NEC CORPORATION, 7-1, Shiba 5-chome Minato-ku, Tokyo, JP
PI EP 831525 A2 19980325
AI EP 1997-116401 19970919
PRAI JP 1996-249969 19960920
ABEN Disclosed is a method for forming a **protruding electrode** which has the steps of: forming a first film of an organic or polymeric material on the **top** portion of a **protruding electrode** formed on a **protruding- electrode**-forming plane; then forming a second film of a polymeric material on the **protruding-electrode** -forming plane to bury the base portion of the **protruding electrode**; and removing the first film after the second film is cured; wherein the first film is of the organic or polymeric material which has no affinity with the polymeric material of the second film.
DETDEN. . . . first film, i.e., the top portion of the protruding electrode since the first film has no affinity with the second **film**. Also, without **conducting** the step of removing the first film, the first film can be automatically removed by heating in the step of. . .
Next, the mask film 16 is removed from the solder bump 14. In this embodiment, the removing of the mask **film** 16 is **conducted** by dissolving the mask film 16 in a solvent by which fluorine system synthetic resin is dissolved and polyimide system. . .
Furthermore, . . . first film, i.e., the top portion of the protruding electrode since the first film has no affinity with the second **film**. Also, without **conducting** the step of removing the first film, the first film can be automatically removed by heating in the step of. . .
CLMEN 1. A method for forming a **protruding electrode**, comprising the steps of:
forming a first film of an organic or polymeric material on the top portion of a **protruding electrode** formed on a **protruding-electrode**-forming plane;
then forming a second film of a polymeric material on said **protruding-electrode**-forming plane to bury the base portion of said **protruding electrode**; and
removing said first film after said second film is cured;
wherein said first film is of said organic. . .
2. A method for forming a **protruding electrode**, according to claim 1, wherein:
said step of removing said first **film** is **conducted** by dissolving said first film into a solvent.
3. A method for forming a **protruding electrode**, according to claim 1, wherein:
said step of removing said first **film** is **conducted** by using ultrasonic cleaning.
4. A method for forming a **protruding electrode**, comprising the steps of:
forming a first film of an organic or polymeric material on the top portion of a **protruding electrode** formed on a **protruding-electrode**-forming plane; and
then forming a second film of a polymeric material on said **protruding-electrode**-forming plane to bury the base portion of said **protruding electrode**;
wherein said first film is of said organic or polymeric material which has no affinity with said polymeric material of. . .
5. A method for forming a **protruding electrode**, according to claim 1, wherein:
said step of forming said first **film** is **conducted** by a printing process using a mask.
6. A method for forming a **protruding electrode**, according to claim 2, wherein:
said step of forming said first **film** is **conducted** by a printing process using a mask.

L49 ANSWER 6 OF 10 EUROPATFULL COPYRIGHT WILA on STN
PATENT APPLICATION - PATENTANMELDUNG - DEMANDE DE BREVET
AN 742643 EUROPATFULL ED 19970307 EW 199646 FS OS Full-text
TIEN An acoustic surface-wave device and its manufacturing method.
IN Onishi, Keiji, 2-2-10, Hitotsuya, Settu-shi, Osaka 566, JP;
PA MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD., 1006, Oaza Kadoma, Kadoma-shi,
PI EP 742643 A1 19961113
PRAI JP 1995-109649 19950508
ABEN The objects of this invention are to offer a compact, low height, low cost, and high reliability acoustic surface-wave device, and its manufacturing method. In order to accomplish the objects of the invention, the invented acoustic surface-wave device is constituted of a substrate (101), comb-electrode (102) disposed on the main surface of said substrate plural electrode pads (103) disposed around said comb-electrode, protecting means (112) covering said comb-electrode through a closed space produced by combining said comb-electrode and said plural electrode pads with said substrate by using substantially covalent bonding force acted between, conductive bumps (104) formed on said plural electrode bumps, a **conductive** adhesive **layer** (105) disposed at least on the **top** of said conductive **bumps**, and a package (107) adhered on said conductive bumps by means of said conductive adhesive, and insulation adhesive filled into said package contacting with said conductive adhesive, said conductive bumps, and said protective means. <image>

CLMEN. . . between said comb-electrode and said plural electrode pads, conductive bumps formed on the tops of said plural electrode pads, a **conductive** adhesive **layer** disposed at least on the tops of said conductive bumps, a package adhered on said conductive bums by means of. . .
1. . . . a protection means (112);
conductive bumps (104) formed on the tops of said plural electrode pads (103);
a **conductive** adhesive **layer** (105) disposed at least on the tops of said conductive bumps (104);
a package (107) adhered on said conductive. . . height of a base of each conductive bump is higher than the height of the protective mans, where each conductive **bump** has a double **protrusion** structure consisting of a top and a base.
6. An acoustic surface-wave device according to Claim 1; wherein said conductive bump consists of a base bonded to said **electrode** pad and a **protrusion** formed on said base where said the height of said base is lower than the height of said protecting means.. . .
6. . . . acoustic surface-wave device according to claim 1, wherein said conductive bump (104) consists of a base (104b) bonded to said **electrode** pad (103) and a **protrusion** (104a) formed on said base (104b), wherein the height of said base (104b) is higher than the height of said. . .
7. . . . comprising; a comb-electrode formed on the main surface of said substrate, plural electrode pads disposed on the peripheral of said comb-**electrode**, an insulating **layer** formed to surround said comb-electrode at an area between said comb-electrode and said plural electrode pads, a protection means covering. . . said comb-electrode and said plural electrode pads, a conductive bumps formed on the tops of said plural electrode pads, a **conductive** adhesive **layer** disposed at least on the tops of said conductive bumps, a package adhered on said conductive bumps by means of. . .
10. . . . (112);
a process to form conductive bumps (104) on said plural electrode pads (103);
a process to form **conductive** adhesive **layer** (105) at least on the tops of said conductive bumps (104);
a process to adhere said conductive bumps (104). . . height of a base of each conductive bump is higher than the height of the protective mans, where each conductive **bump** has a double **protrusion** structure consisting of a top and a base,
14. An acoustic surface-wave device according to Claim 7; wherein said conductive bump consists of a base bonded to said **electrode** pad and a **protrusion** formed on said base, and the height of said base is lower than the height of protecting means.
15. . . . said plural electrode pads, a process to form conductive bupms on said plural electrode pads, a process to form a **conductive** adhesive **layer** at least on the tops of said conductive bumps, a process to adhere said conductive bumps on to said electrode. .

L49 ANSWER 8 OF 10 EUROPATFULL COPYRIGHT WILA on STN

PATENT APPLICATION - PATENTANMELDUNG - DEMANDE DE BREVET

AN 316912 EUROPATFULL ED 20000924 EW 198921 FS OS STA B Full-text
TIEN A bump electrode structure of a semiconductor device and a method for forming the same.
IN Wakabayashi, Takeshi Pat. Dpt. Dev. Div Hamura R&D, Center Casio
PI EP 316912 A2 19890524
PRAI JP 1987-289257 19871118
JP 1987-294133 19871124
JP 1988-105302 19880427

ABEN A bump electrode structure of a semiconductor device comprises an electrode pad (13) formed of an alu.shy. minum alloy, an insulating oxide layer (14) covering only the peripheral edge portion of the electrode pad (13), an under-bump layer (15) formed of an alloy of titanium and tungsten, and a bump electrode (16) formed of gold. The titanium-tungsten alloy functions both as a barrier metal and as a bonding metal. The bump electrode (16) rises substantially straight from the bonding surface of the under-bump layer (15), and its top portion has an area only substantially equal to that of the electrode pad (13). Fine V-shaped grooves (17) are formed on the **top** surface of the **bump** electrode (16) by anisotropic etching. Thus, the semiconductor device with fine electrode pad pitches is provided with a high-.shy. reliability bump electrode structure which ensures suf.shy. ficient bonding strength between internal and external electrodes.

. DETDEN. . . 5a is formed on bonding metal layer 4b. Using bump electrode 5 as a mask, thereafter, that portion of under-bump **layer** 4 outside **electrode** 5 is removed by etching, as mentioned before. Usually, isotropic wet etching is used for this purpose.
In . . . edge portion of the under-bump layer being situated between the respective peripheral edge portions of the opening of the insulating **layer** and the **electrode** pad; and a protu.shy. berant bump electrode bonded to the under-bump layer and raised from the peripheral edge portion of. . .
Fig. . . . inter.shy. mediate junction layer 15 is situated between the outer end of electrode pad 13 and opening 14a of insulating **layer** 14. Bump **electrode** 16 of gold is projectingly formed on **layer** 15. **Electrode** 16, which is composed of thin gold layer 16a and gold bump 16b, has an overall thickness of about 10. . .

CLMEN. . . being situated between the respec.shy. tive peripheral edge portions of the opening (14a) of the insulating layer (14) and the **electrode** (13); and
a **protuberant bump electrode** (16)
bonded to the under-bump (15) and raised from the peripheral edge portion of the under-bump layer (15).
5. 5. A method for forming a bump electrode of a semiconductor device so that the **bump electrode** (16) **protrudes** from the upper surface of an electrode pad (13) whose central portion of is exposed through an opening (14a) of. . .